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AMENDED CLAIMS

1. (original) A method of improving the efficiency of a synchronous mirror delay circuit comprising:

providing a clock input signal (CIN), an inverted clock input signal (CIN') and a clock delay signal (CDLY);

detecting a plurality of phases of CIN and CDLY based on timing conditions associated with CIN and CDLY; and

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selectively inputting CIN or CIN' into ~~a~~ the synchronous mirror delay circuit (SMD) based on the phase of CIN and CDLY to reduce a number of required delay stages in the SMD.

2. (original) The method of claim 1 wherein the timing conditions include a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}) and wherein the selectively inputting step includes inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$ and inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ to reduces the number of required delay stages in the SMD.

3. (original) The method of claim 2 wherein the number of delay stages in the SMD is reduced substantially in half.

4. (original) The method of claim 2 wherein the SMD has a plurality of delay lines and wherein the number of delay stages in at least one of the SMD delay lines is reduced substantially to 59 from 128.

5. (original) A method of improving the efficiency of a synchronous mirror delay circuit comprising the steps of:

providing a clock input signal (CIN), an inverted clock input signal (CIN') and clock delay signal (CDLY), each signal having timing characteristics;

interposing a phase detector and selection system between an external clock signal and ~~a~~ the synchronous mirror delay circuit;

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determining which of a number of phases the signals are ~~in~~ based on the timing characteristics; and

selectively directing the signals based upon the phase of the signals.

6. (original) The method of claim 5 wherein the selectively directing step includes selectively directing CIN or CIN' to the synchronous mirror delay based upon the timing characteristics of CIN and CDLY.

7. (original) The method of claim 5 wherein the selectively directing step includes bypassing CIN or CIN' from the synchronous mirror delay based upon the timing characteristics of CIN and CDLY.

8. (original) The method of claim 5 further including defining the timing characteristics as a period of CIN as t_{ck} and defining a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein the determining steps includes determining that the phases include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$;

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a fourth phase when $t_{mdl} = t_{ck}/2$.

9. (original) A method of reducing a number of effective delay stages in a synchronous mirror delay (SMD), the method comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN') and a clock delay signal (CDLY) having timing characteristics;

differentiating, with a phase detector, a plurality of phases based upon the timing characteristics of CIN and CDLY; and

selecting, based on the phases, one of CIN and CIN' to be input into ~~a~~ the synchronous mirror delay, thereby reducing the effective delay stages in the SMD.

10. (original) A method of reducing a number of effective delay stages in a synchronous mirror delay (SMD), the method comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN') and a clock delay signal (CDLY) having timing characteristics;

determining a plurality of phases based upon the timing characteristics of CIN and CDLY;

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for at least one phase, directing CIN' into the synchronous mirror delay such that a reduced number of delay stages are achieved.

11. (original) The method of claim 10 wherein the timing characteristics define a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein the directing step occurs when $t_{mdl} < t_{ck}/2$.

12. (currently amended) ~~The method of claim 11, further including the steps of:~~

~~multiplexing an input with an input selection multiplexor to select whether to direct the CIN or CIN' into the SMD, based on the phase determined in the determining step; and~~

~~multiplexing, with an output selection multiplexor, an output of the input selection multiplexor with an SMD output, the output selection multiplexor selecting whether to output, based on the phase determined in the determining step, the SMD output or CIN bypassing the SMD, as an input to a clock tree to generate an internal clock signal.~~

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A method of reducing a number of effective delay stages in a synchronous mirror delay (SMD), the method comprising:

a) providing an internal clock signal (CIN), an inverted internal clock signal (CIN'), and a clock delay signal (CDLY) having timing characteristics;

b) determining a plurality of phases based upon the timing characteristics of CIN and CDLY;

c) for at least one phase, directing CIN' into the SMD such that a reduced number of delay stages are achieved;

wherein the timing characteristics define a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein the directing step occurs when $t_{mdl} < t_{ck}/2$;

d) multiplexing an input with an input selection multiplexor to select whether to direct the CIN or CIN' into the SMD, based on the phase determined in the determining step; and

e) multiplexing, with an output selection multiplexor, an output of the input selection multiplexor with a SMD output, the output selection multiplexor selecting whether to output,

based on the phase determined in the determining step, the SMD output or CIN bypassing the SMD, as an input to a clock tree to generate an internal clock signal.

13. (original) A memory device comprising:

a synchronous mirror delay (SMD) circuit; and

a phase detector connected to the SMD, the phase detector receiving a clock input signal and a clock delay signal, the clock input signal (CIN) and the clock delay signal (CDLY) each having timing characteristics, the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality of conditions of the clock input signal and the clock delay signal based on the timing characteristics, and wherein at least one of the conditions reduces a number of effective delay stages in the SMD.

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14. (original) The circuit of claim 13 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and

wherein a first phase is when $t_{mdl} > t_{ck}/2$;

wherein a second phase is when $t_{mdl} < t_{ck}/2$;

wherein a third phase is when $t_{mdl} = t_{ck}$; and

wherein a fourth phase is when $t_{mdl} = t_{ck}/2$.

15. (original) The circuit of claim 14 wherein when $t_{mdl} < t_{ck}/2$ the number of effective delay stages in the SMD is comparable to when $t_{mdl} > t_{ck}/2$.

16. (original) The circuit of claim 14 wherein the number of effective delay stages when $t_{mdl} < t_{ck}/2$ is reduced by substantially one-half.

17. (original) The circuit of claim 14 wherein the number of effective delay stages when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

18. (original) A synchronous mirror delay system comprising:

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a synchronous mirror delay (SMD); and

a phase detector associated with the SMD, the phase detector receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and the CDLY each having timing characteristics, the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality of conditions based on the timing characteristics of CIN and CDLY, and wherein at least one of the conditions reduces the number of effective delay stages in the SMD;

wherein the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein the plurality of conditions include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$;

wherein the number of effective delay stages in the second phase is reduced; and

wherein in the third and fourth phases, CIN bypasses the SMD.

19. (currently amended) A synchronous mirror delay circuit for use with an external clock signal comprising:

an input buffer having an input ~~connected to~~ for receiving the external clock signal and an output ~~connected to~~ related to a clock input signal (CIN), an inverted clock input signal (CIN') and a clock delay signal (CDLY) each having timing characteristics;

a synchronous mirror delay (SMD) having a measurement delay line input for connection to a measurement delay line, a measurement delay line output connected to a variable delay line input for connection to a variable delay line, the variable delay line including a variable delay line output; and

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a phase detector disposed between the input buffer and the ~~synchronous mirror delay~~ SMD, the phase detector having a first input for receiving the CIN, a second input for receiving the CDLY, the phase detector generating one of a plurality of output signal combinations, each combination corresponding to a phase of the CIN and CDLY signals based on the timing characteristics, a CDLY SMD input connected to the measurement delay line input, and ~~an~~ a SMD output connected to the variable delay line output, ~~the~~ a circuit selectively inputting CIN or CIN' as a CIN SMD input based on the phase of the signals, and wherein at least one of the phases reduces a number of effective delay stages of the SMD.

20. (original) The circuit of claim 19 wherein the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein when $t_{mdl} < t_{ck}/2$, CIN' is input into the SMD and when $t_{mdl} > t_{ck}/2$ CIN is input into the SMD.

21. (original) The circuit of claim 20 wherein the number of effective delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced.

22. (original) The circuit of claim 20 wherein the number of effective delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

23. (original) A synchronous mirror delay system comprising:

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a synchronous mirror delay (SMD); and

a phase detector in operational association with the SMD, the phase detector receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and the CDLY each having timing characteristics, the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality of conditions based on the timing characteristics, and wherein a number of effective delay stages of the SMD is reduced.

24. (original) The system of claim 23 wherein under one condition the number of effective delay stages is reduced by substantially one-half .

25. (currently amended) The system of claim 23 wherein the timing characteristics ~~defines~~ define a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein the plurality of conditions include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$; and

wherein in the second phase, the number of effective delay stages of the SMD is reduced.

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26. (currently amended) A phase detection and selection circuit comprising:

a phase detector for receiving a clock input signal (CIN)~~, an inverted clock input signal (CIN')~~ and a clock delay signal (CDLY), each signal having timing conditions, and generating a plurality of output signal combinations, each combination based upon the timing conditions; and

logic associated with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals; and

wherein ~~the~~ a phase detection and selection system selectively feeds CIN or an inverted clock input signal (CIN') ~~CIN'~~ into a synchronous mirror delay upon which the plurality of output signal combinations is generated and wherein a number of effective delay stages is reduced.

27. (original) The circuit of claim 26 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and wherein the phases include:

a first phase when $t_{mdl} > t_{ck}/2$; and

a second phase when $t_{mdl} < t_{ck}/2$; and

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$.

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28. (original) The circuit of claim 27 wherein the number of effective delay stages is reduced.

29. (original) The circuit of claim 27 wherein number of effective delay stage is reduced substantially by one-half.

30. (original) The circuit of claim 27 wherein the number of effective delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

31. (canceled)

32. (canceled)

33. (canceled)

34. (original) A system comprising:

a processor;

a memory controller;

a plurality of memory devices;

a first bus interconnecting the processor and the memory controller;

a second bus interconnecting the memory controller and the memory devices;

each of the memory devices having:

a synchronous mirror delay (SMD) circuit;

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a phase detector for receiving a clock input signal (CIN) and a clock delay signal (CDLY), each signal having timing conditions, and generating a plurality of output signal combinations, each combination corresponding to phases of the signals based upon the timing conditions; and

logic associated with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals; and

wherein the timing conditions include a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}) and wherein inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$ and inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ reduces a number of delay stages in the SMD.

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